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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,213	12/20/2001	Richard Slobodnik	550-298	6125

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,213	SLOBODNIK, RICHARD	
	Examiner	Art Unit	
	John J Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been examined.

Specification

2. The specification is objected to because of the following informalities: Misspelling of customization on page 4, line 12. Appropriate correction is required.

3. The abstract of the disclosure is objected to because of improper placement of "[Figure 5]" and should be removed. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claim 6 objected to because of the following informalities: The claim should read: "...a processor core; wherein said processor core...". Appropriate correction is required.

5. Claim 6 is objected to because of lack of line indentation according to 35 CFR 1.75(i).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 4, 5, 7, 8, and 11-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4 and 11:

These claims are unclear because the limitation used "at least one memory" implies one memory or more, and "synthesized and a custom memory" always implies more than one. The two are inconsistent and renders the claims indefinite. For reason of examination the Examiner is reading this to imply "synthesized or a custom memory".

Claims 5 and 12:

The term "adapted" is unclear and, therefore, renders the claim indefinite. It is not clear how the memory is adapted. Also "adapted" is not positive limitation.

Claims 7 and 14:

These claims are not clear and do not appear to further limit claims 1 and 8, respectively.

Claim 8:

This claim sites the limitation "A method of testing a memory". Line 5 states "at least one memory". This is inconsistent with the preamble stating a memory and renders the claims indefinite. Therefore, line 5 should read: "said memory".

Claims 11-13:

These claims are rejected because they depend on claim 8 and contain the same problems of indefiniteness. As a result, all occurrences of "said at least one memory" should read "said memory".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 3, 4, 6, 8, 10, 11,13 are rejected under 35 U.S.C. 102(e) as being anticipated by Gold (US-2003/0167428).

Claims 1 and 8:

Gold teaches electronic device 10 includes a BIST engine 20 (self-test controller) that generates a test vector for a physical memory row address of the embedded memory 28 (memory). Gold also teaches a memory address converter 24 Mapping circuit) that converts the physical address generated by the BIST engine 20 to a corresponding logical address in the embedded memory 28. (Page 2, ¶ 17).

Claims 3 and 10:

Gold teaches the BIST engine 20 (controller) generates the physical memory address 34 (first physical address) and the adjacent physical memory address 36 (second physical address). The BIST engine 20 passes the physical memory address 34 and the physical memory address 36 to the address converter 24 (mapper). The address converter 24 (mapper) maps the physical memory address 34 (first physical address) to the corresponding logical memory address 40 (first logical address), and maps the physical memory address 36 (second physical address) to the corresponding

logical memory address 42 (second logical address). The test vectors generated by the BIST engine 20 are then written to the logical memory addresses of the embedded memory array 28. (Page 2, ¶ 23).

Claims 4 and 11:

Gold teaches electronic device 10 includes a BIST engine 20 (self-test controller) that generates a test vector for a physical memory row address of the embedded memory 28 (synthesized memory).

Claim 6:

Gold teaches an integrated circuit that contains a memory array (memory) and a test generator (controller) coupled to the memory array to generate a physical address of the memory array and a corresponding test vector. (Page 1, ¶ 10). Gold also teaches the method for testing an embedded memory has a microprocessor. (Page 2, ¶ 16).

Claim 13

Gold teaches the microprocessor (processor core) performs BIST on a memory array (memory) having a physical address map distinct from its logical address map. (Page 2, ¶ 16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gold (US-2003/0167428).

Claims 5:

Gold does not explicitly teach "said mapping circuit is part of an interface circuit", however, Gold does suggest the address converter 24 (mapping circuit) may be adapted to support built-in self-repair of the embedded memory array 28 (at least one memory). (Page 2, ¶ 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Gold's address converter 24 (mapping circuit), in being adapted to support built-in self-repair of the embedded memory array 28 would contain the necessary circuitry to synchronize the timing of the signals connected to the memory array 28. The artisan would be motivated to believe so because built-in self-repair circuits inherently adapt the repair circuit to the memory timing it is repairing through synchronization of the signals interfacing to the memory array. In this way the interface circuit of the instant application would already be included in Gold's address converter 24 (mapping circuit).

Claims 7 and 14:

Gold does not explicitly teach "a plurality of memories, a mapping circuit being provided for each of said memories", however, Gold does teach the memory address converter 24 (mapping circuit) converts the physical address generated by the BIST engine 20 (controller) to a corresponding logical address in the embedded memory 28 (memory). (Page 2, ¶ 17). Gold also suggests that the electronic device 10 can include more than one data bus. (Page 2, ¶ 24). It would have been obvious to one of ordinary

skill in the art at the time the invention was made that Gold's electronic device 10 can be modified to comprise of a plurality of memories and memory address converter circuits. The artisan would be motivated to do so to enable the mapping of the physical address to the logical address of multiple memories.

9. Claims 2, 9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gold (US-2003/0167428) and further in view of Patti (US-6469945).

Claims 2 and 9:

Gold does not explicitly teach the physical address signals include row and column address signals, however, Gold does teach a BIST engine 20 (self-test controller) that generates a test vector for a physical memory row address of the embedded memory 28 (memory). (Page 2, ¶ 17). Gold also teaches the address converter 24 (mapping circuit) may be adapted to support built-in self-repair of the embedded memory array 28. (Page 2, ¶ 21). In addition, Gold suggests the address converter 24 (mapping circuit) can be any conventional type of solid state memory device, such as a read only memory (ROM), a random access memory (RAM), an electronically erasable programmable read only memory (EEPROM), or the like. (Page 2, ¶ 17). Patti teaches that controller 40 loads physical row and column addresses into row/column address CAM 43 and 42. Patti teaches controller 40 alters the mapping in CAM 43 and 42 when a bad row or column is found such that the bad row or column is replaced by one of the spares. (See col. 4, lines 4-8). Patti's suggests the mapping circuit utilizes a CAM to map the physical address within the memory chip, i.e., rows and columns in the storage array, to the logical addresses, however, the mapping circuit

can include some form of non-volatile memory such as EEPROM or FLASH in which the mapping is stored when power is turned off. (See col. 9. lines, 9-18). As previously stated, Gold also teaches the mapping circuit can include an EEPROM or FLASH. (Page 2, ¶ 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Gold's BIST engine 20 could be modified with Patti's controller to generate physical column address as well as physical row addresses. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gold's address converter 24 (mapping circuit) to include a column ROM or EEPROM or FLASH memory as in Patti's mapping circuit. The artisan would be motivated to do so because it would enable Gold to test or replace the memory array 28 columns as well as the rows.

Claim 12:

Gold does not explicitly teach "said mapping circuit is part of an interface circuit", however, Gold does suggest the address converter 24 (mapping circuit) may be adapted to support built-in self-repair of the embedded memory array 28 (at least one memory). (Page 2, ¶ 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Gold's address converter 24 (mapping circuit), in being adapted to support built-in self-repair of the embedded memory array 28 would contain the necessary circuitry to synchronize the timing of the signals connected to the memory array 28. The artisan would be motivated to believe so because built-in self-repair circuits inherently adapt the repair circuit to the memory timing it is repairing through synchronization of the signals interfacing to the memory array. In this way the

interface circuit of the instant application would already be included in Gold's address converter 24 (mapping circuit).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJT

Guy J. Lamarre
for

Albert DeCady
Primary Examiner